

11. (Original) The circuit of Claim 8,
wherein the parameter adjustment circuit includes:
a first digital-to-analog converter circuit that is configured to convert the count signal into a first analog signal; and
a second digital-to-analog converter circuit that is configured to convert an inverted count signal into a second analog signal.
12. (Original) The circuit of Claim 11, wherein
the coarse channel circuit includes an amplifier that is configured to provide a differential output current,
the amplifier includes:
a first load that is configured to receive a first half of the differential output current and the first analog signal; and
a second load that is configured to receive a second half of the differential output current and the second analog signal,
the first current digital-to-analog converter circuit is configured to provide the first analog signal to the first load, and wherein
the second current digital-to-analog converter circuit is configured to provide the second analog signal to the second load.
13. (Original) The circuit of Claim 12, wherein
the first current digital-to-analog converter circuit includes:
a first current digital-to-analog converter; and
a first transistor that is coupled between the first current digital-to-analog converter and the first load,
the second current digital-to-analog converter circuit includes:
a second current digital-to-analog converter; and

a counter circuit that is configured to provide a count signal in response to the timing signal and the output signal; and

a parameter adjustment circuit that is configured to adjust the parameter in response to the count signal.

18. (Original) A method for coarse channel calibration in a folding analog-to-digital conversion architecture, the method comprising:

providing a reference voltage to a coarse channel circuit of a folding analog-to-digital converter circuit; and

adjusting a parameter of the coarse channel circuit until an output of the coarse channel circuit is calibrated in relation to the reference voltage.

19. (Original) The method of Claim 18, further comprising:

receiving a signal from the coarse channel circuit after providing the reference voltage; and
adjusting a count in response to the signal,
wherein the parameter is adjusted according to the count.

20. (Original) A circuit with an analog-to-digital conversion architecture, comprising:
means for providing a fine channel circuit with a folding analog-to-digital converter architecture;

means for providing a coarse channel circuit; and

means for calibrating the coarse channel circuit.

21. (New) The circuit of Claim 1, wherein

the fine channel circuit is arranged to perform a fine analog-to-digital conversion of an input signal; and

wherein the coarse channel circuit is arranged to perform a coarse analog-to-digital conversion of the input signal in parallel with fine analog-to-digital conversion.

22. (New) The circuit of Claim 1, wherein

the coarse channel circuit is arranged to perform a coarse analog-to-digital conversion; and
wherein the coarse channel calibration circuit is arranged to calibrate the coarse analog-to-digital conversion.

23. (New) The circuit of Claim 1,
wherein the coarse channel circuit includes an amplifier array.
24. (New) The circuit of Claim 4,
wherein the coarse channel calibration circuit is configured to:
 receive a feedback signal from the coarse channel circuit, and
 provide the adjustment signal to the coarse channel circuit in response to the
feedback signal.
25. (New) The circuit of Claim 15, further comprising:
 a fine channel circuit that is arranged to perform a fine analog-to-digital conversion of an
input signal in parallel with a coarse analog-to-digital conversion of the input signal performed by
the coarse channel circuit.